Microwave Planar Active Filters in GaAs and SiGe Technologies

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Abstract — **This paper deals with the design of integrated planar active filters on Si and GaAs substrates. Implementation techniques are detailed in both technologies for active LC filters. A comparison between the two technologies is made with the design of integrated negative resistance circuits.**

I. INTRODUCTION

Due to great advances of Silicon, and Silicon-Germanium technologies during the last decade, Silicon-based ICs have found an increasing importance for RF applications [1]. The SiGe BiCMOS HBT is the name given to heterojunction bipolar transistor, for which the base is doped with Germanium. Using this technology, the chip works much faster while ensuring the reliability and the stability of such process. These chips can be designed for wireless applications, increasing the performance of these products while decreasing their size and power consumption. Besides, the BiCMOS HBT SiGe technology takes advantage of the integration capability of CMOS process that leads to more compactness.

The objective of this paper is first to show applications of GaAs and SiGe technologies for active filtering functions. Then, a comparison is made with the implementation of negative resistances to emphasize the promising advantage of SiGe vs. GaAs in terms of compactness and cost. We also discuss differences from the designer point of view in terms of component implementation and availability in both technologies.

II. DESIGN PROBLEMS AND CONSTRAINTS

During the last three decades, the use of Silicon technology was restricted to low frequency digital and analog applications. Recently, the number of articles reporting the use of SiGe technology for RFIC design has increased. According to the comments held during the discussions at the IMS'2000 conference in Boston [2], there are still various opinions on the advantages and drawbacks of one or the other technology.

There are two different ideas on the issue of using SiGe technology. On the one hand, Si and SiGe technologies are found very advantageous, due to their capability to achieve hand, the degree of maturity of Si/SiGe technologies is still not comparable to that of GaAs technologies. According to some designers, Si technology does not enable integration of a complete microwave system. It may then be necessary to use mixed technologies, which tends to be more expensive than a complete development on GaAs.

With the same idea, the same arguments also confront designers about SOP techniques (System-On-Package) [3]. Anyway, in spite of obvious advantages of cost effectiveness and compactness of circuits designed using SiGe technology, there seem to be some constraints, among which the more important is the lack of proper library model in conventional microwave and high frequency circuit simulators. To become more familiar with Si and SiGe technologies, and before confronting with the realization of circuits, we have tested several processes through their design kits. The first major problem is encountered at the level of the CAD tools. Because of the classical use of silicon technology for digital and analog applications at low frequencies, most part of these libraries are naturally developed for CAD software using the same approach. The design philosophy of these circuits is very far from that used for microwave analog circuits.

The second problem arises from the fact that some component models are not available in simulator libraries or not parameterized, thus making any optimization a hard task. As a result, some components like inductors are not available, because they are not classically used at low frequencies. In some processes, it is also the case for varactor diodes.

From the design point of view, the third problem comes from the specific conductivity of the doped Silicon (SiGe) substrate and its bad isolation (some tenths of ohms.cm compared to 10^5 ohm.cm for pure silicon). This leads to considerable increase in the number of parasitic capacitors in a circuit. For example, in the case of the MOSFET, it is necessary to take into account not only the parasitic capacitors C_{gs} and C_{gd}, but also capacitors C_{db}, C_{bs} and C_{gb} (parasitic capacitors between the substrate and respectively the drain, the source and the gate). These capacitances are non-negligible regarding the other capacitances of the

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For the same reason, components such as inductors perform very low quality factor ($Q \leq 5$) and make them unusable. The design rules in the two technologies are also very different, even for the design of simple circuits. For technological reasons, the ground plane of a circuit on silicon is located on the top of the substrate. It is then not possible to strictly consider microstrip lines. However, recent works have shown the feasibility of transmission lines in polymers, such as BCB allowing performances close to those obtained with GaAs [1]. A particular attention should be also paid to the leakage currents due to the specific conductivity of the substrate. To solve this problem, many manufacturers use guard rings. These guard rings are buried layers, surrounding partially or totally the component to be protected by acting as PN junction biased in inverse. All these protection processes clearly allow a more compact implementation in comparison to GaAs, leading to very different design rules and components placement than those applied for conventional microwave GaAs technology. This mainly explains differences in size that can be observed for the same function from one technology to the other.

III. Realization Examples

Here, we present the comparative characteristics of two active functions realized in SiGe and GaAs technologies.

A. Negative Resistance-Based Active Filter

The topology of negative resistance used is derived from ideal negative impedance converters classically employed at low frequencies. The approach consists in replacing the ideal impedances of the circuits with lumped components networks to compensate for the effects of the parasitics of active and passive MMIC elements. Moreover [4], transistor devices are replaced by cascade topology to realize high value equivalent transconductances as needed by this topology. This cascade configuration also permits to use simpler matching networks [5].

Using this approach, we synthesize a negative resistance around 4 GHz. The basic topology of the filter is presented in figure 1. Coupled lines are used at the input and output of the circuit to decouple the LC active resonator and control the filter selectivity. With this topology, we can compensate for the losses of the passive inductor, then of the LC shunt resonator and finally of the global filter. We present in figure 2 the layout of this filter. The simulated results for a quality factor of about 1000 are presented in figure 3.

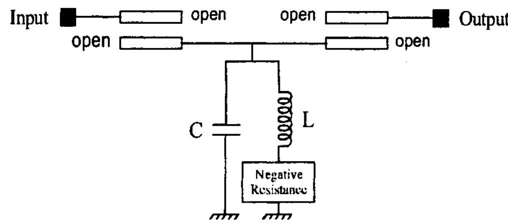

Fig. 1. Basic LC shunt bandpass filter topology

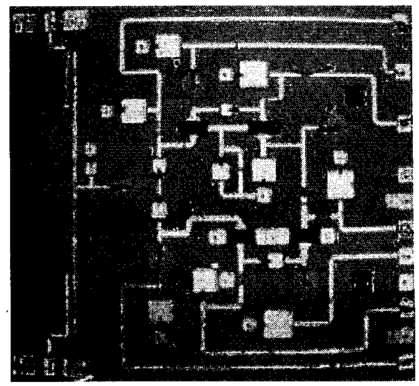

Fig. 2. Photography of the LC filter

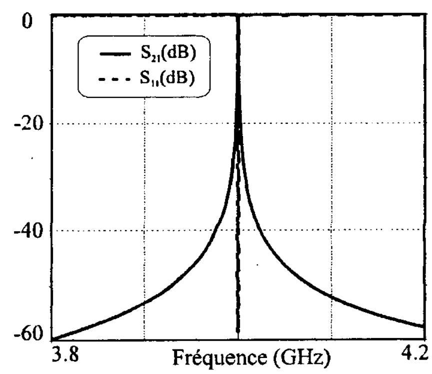

Fig. 3. S-parameters response

B. Active Inductance LC Filter

Based on the topology proposed in [6], [7] for InAlAs/InGaAs HBT technology, we propose a grounded active inductor using a low cost 0.8 μm BiCMOS HBT technology [8]. This inductor topology is based on the use of two HBTs in a feedback configuration. Note that in this case there is no need of integrated inductor (figure 4).

Q_1 is biased by a voltage-controlled current source classically used with bipolar transistors.

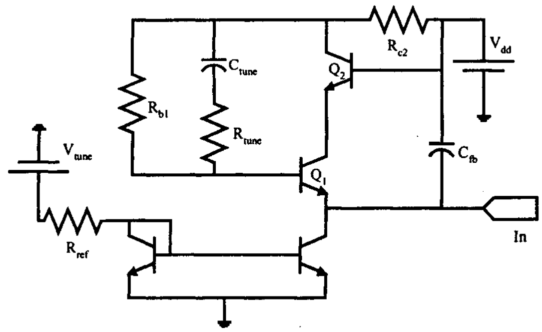

Fig. 4. Schematic of the active inductor

V_{tune} allows tuning of the associated real part while maintaining the inductive impedance. Using this approach, a quality factor of some thousands can be performed for an inductance value of 9.20 nH. By associating a capacitor in parallel with the active inductance a bandpass response can be also obtained. The active LC resonator is decoupled thanks to two small value capacitors. We present in figure 5 the layout of the filter and in figure 6 the simulated results, taking into account the parasitic capacitances due to the Si substrate conductivity.

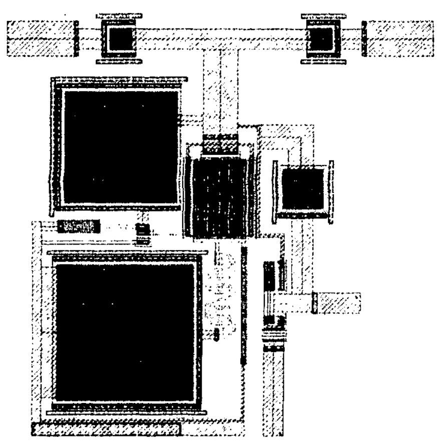

Fig. 5. Layout of the integrated active LC filter in BiCMOS HBT technology

Dimensions of this circuit are 150x170 μm². Total consumption is about 15 mW. We obtain a bandpass filter which losses are totally compensated at 1.86 GHz, with a quality factor of about 150 at f_0.

C. Negative Resistances

Two different negative resistor topologies are discussed and compared. The first circuit uses a BiCMOS SiGe HBT technology.

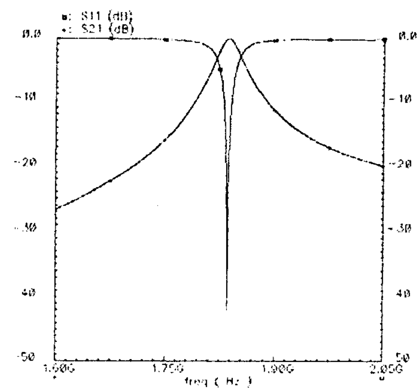

Fig. 6. Layout-based LC filter simulated results

A differential structure is used here. Such topologies generally present a real part of the impedance not strongly frequency-dependent and are recommended for wideband applications [9]. Another important point is that such devices seem insensitive to noise. Moreover, linearization methods classically applied for transconductors stages can also be used. The schematic of the circuit is presented in figure 7 and the layout in figure 8. Three integrated inductors are used to bias and stabilize HBTs. A current source sets the emitter current. Symmetric performances are obtained between the two ports. The imaginary part can be considered as a negative capacitance.

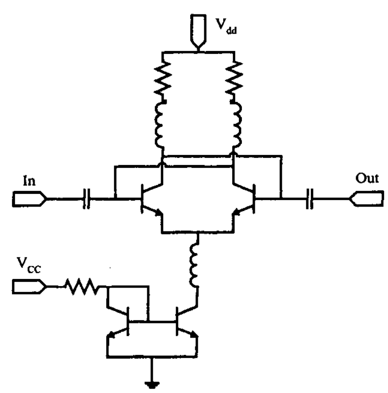

Fig 7. Schematic of the differential negative resistance

Circuit dimensions are 690x800 μm². The negative resistance performed is about -10 Ω at 1.8 GHz. The imaginary part is equivalent to a -2.4 pF negative capacitance that can also be used to design a gyrator [5].

The GaAs version of the second negative resistance has been realized using the HEMT ED02Ah process of OMMIC [10].

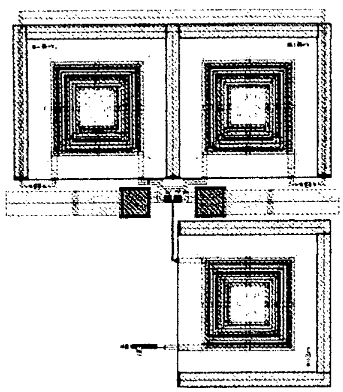

Fig. 8. Layout of the differential negative resistance

This one-port circuit uses three transistors in a feedback configuration as shown in figure 9 and figure 10. The transistors are biased through LC cells for the drain, and high values resistors for the gates. The negative resistance performed is about -12 Ω in the [1.9 - 2.3 GHz] range. The associated imaginary part is equivalent to a LC series resonator (L=4 nH, C=0.5 pF). Circuit size is 1.5x2 mm².

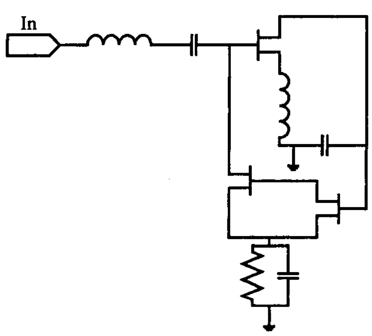

Fig 9. Schematic of the grounded negative resistance

To try to highlight one technology with regards to the other one, we now give some general elements of comparison:

- the surface ratio between SiGe and GaAs is about 5,
- the corresponding cost ratio is about 7,
- the power consumption ratio is about 4 (46 mW in SiGe against 73 mW in GaAs).

Those results clearly seem to give advantage to SiGe technology in term of size, cost and power consumption. Note that another important point also resides in the fact that in circuits using bipolar transistors, the designer must be familiar with particular biasing methods and topologies which clearly complicates the design procedure.

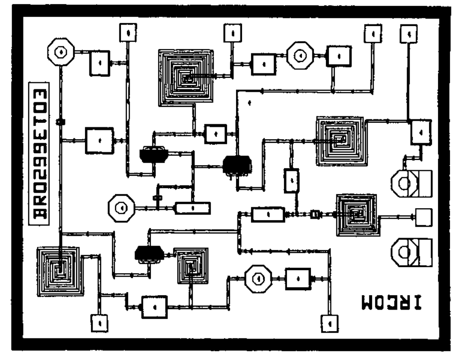

Fig. 10. Layout of the grounded negative resistance

All these elements tends to confirm what was said two years ago in Boston [2] and even if SiGe technology is obviously promising, GaAs technologies still provide many advantages, would it only be in term of technological maturity.

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